

What is claimed is:

1 1. A method for forming an interconnect structure comprising:
2 forming a first dielectric layer over a conductive layer using chemical vapor
3 deposition;
4 forming a second dielectric layer over said first dielectric layer by spin coating;
5 via etching said second dielectric layer and said first dielectric layer to form a via
6 opening extending through said second dielectric layer and said first dielectric layer ;
7 filling said via opening with a plug material; and
8 trench etching said second dielectric layer and said plug material to form a trench
9 over a lower portion of said via opening and to remove said plug material from said via
10 opening, thereby forming a dual damascene opening.

1 2. The method as in claim 1, wherein each of said first dielectric layer and
2 said second dielectric layer comprise low-k dielectric materials.

1 3. The method as in claim 1, wherein said plug material comprises
2 photoresist.

1 4. The method as in claim 1, wherein said plug material comprises a spin-
2 on low-k dielectric material.

1 5. The method as in claim 4, wherein said second dielectric layer is a low-
2 k dielectric material that is the same as said spin-on low-k dielectric material.

1 6. The method as in claim 5, wherein said first dielectric layer and said
2 spin-on low-k dielectric material have different etch rates during said trench etching.

1 7. The method as in claim 1, wherein said first dielectric layer and said
2 second dielectric layer have different etch rates during said trench etching.

1 8. The method as in claim 1, wherein said first dielectric layer is
2 substantially resistant to being etched during said trench etching.

1 9. The method as in claim 1, wherein said first dielectric layer and said
2 second dielectric layer have an etch selectivity no less than 20:1 in said trench
3 etching.

1 10. The method as in claim 1, wherein said trench etching includes at least
2 one of H₂, N₂, Ar and O₂ as an etch gas.

1 11. The method as in claim 1, wherein said trench etching includes using
2 only H₂, N₂, Ar and O₂ as etch gases.

3 12. The method as in claim 1, wherein said filling comprises coating said
4 plug material over said second dielectric layer and filling said via opening, and one
5 of polishing and etching back said plug material.

1 13. The method as in claim 1, further comprising forming an antireflective
2 coating layer over said plug material and said second dielectric layer after said filling.

1 14. The method as in claim 1, further comprising forming a further layer
2 over said second dielectric layer prior to said via etching and in which said via
3 etching further comprises etching said further layer, said further layer comprising at
4 least one of a hardmask and an anti-reflective coating.

1 15. The method as in claim 1, wherein said forming a first dielectric layer
2 over a conductive layer further comprises forming an etch stop layer over said
3 conductive layer and forming said first dielectric layer on said etch stop layer, and
4 further comprising etching said etch stop layer after said trench etching.

1 16. The method as in claim 1, wherein said first dielectric layer has a
2 dielectric constant no greater than 3.0 and is one of HBD, an oxide and an ultra low-
3 k dielectric material having a dielectric constant less than 2.5.

1 17. The method as in claim 1, wherein said second dielectric layer has a
2 dielectric constant no greater than 2.6 and is one of SiLK and porous SiLK.

1 18. The method as in claim 1, further comprising forming a cap layer on
2 said first dielectric layer and in which said forming a second dielectric layer
3 comprises forming said second dielectric layer on said cap layer and said via etch
4 further comprises etching said cap layer.

1 19. The method as in claim 18, wherein said forming a cap layer
2 comprises forming a layer of one of SiC, SiN, SiCN, SiOC and SiON.

1 20. The method as in claim 18, wherein said cap layer is substantially
2 resistant to being etched during said trench etching.